## CLAIMS

What is claimed is:

1. A method for reducing power consumption of at least one processor in a system, the processor is associated with at least one queue for storing instructions for execution by the processor, the method comprising:

analyzing instructions stored in the queue;

determining a load estimation based on in part a result of the analyzing;

selecting a clock rate out of a plurality of clocking rates based on in part the determined load estimation; and

clocking the processor at the selected clock rate.

2. The method of claim 1, wherein the analization result comprises a determination of the number of the queued instructions.

3. The method of claim 1, wherein the analization result comprises a determination of processing required by each queued instruction.

4. The method of claim 1, wherein the load estimation is based on in part a temperature of the microprocessor.

5. The method of claim 1, wherein at least one processor means having two microprocessors in the system, a first microprocessor is for general purpose and a second processor is for graphic processing purpose, the method comprising:

queuing all instructions at a first instruction queue;

distributing non graphic related instructions to be queued at a second instruction queue where said first microprocessor executes queued instructions from; and

distributing graphic related instructions to be queued at a third instruction queue where said second microprocessor executes queued instructions from.

6. The method of claim 1, wherein at least one queue for storing instructions means having two queues, the method comprising:

queuing instructions at a first instruction queue and distributing instructions queued at said first instruction queue to a second instruction queue where said processor executes the queued instructions from.

7. The method of claim 6, wherein determining a load estimation further comprising using the first number of instructions queued at said first instruction queue and the second number of instructions queued at said second instruction queue as separate control factors.

8. A system having means for reducing power consumption of at least one processor, the processor is associated with at least two queues for storing instructions for execution by the processor, the system comprising:

means for queuing instructions at a first instruction queue;

means for distributing instructions queued at said first instruction queue to a second instruction queue where said processor executes the queued instruction from;

means for analyzing instructions stored in the queues;

means for determining a load estimation based on in part a result of the analyzing;

means for selecting a clock rate out of a plurality of clocking rates based on in part the determined load estimation; and

means for clocking the processor at the selected clock rate.

9. The system of claim 8, wherein means for instructions queued in said first instruction queue and the instructions queued in said second instruction queue as separate control factors.

10. The system of claim 8, wherein at least one processor means having two microprocessors in the system, a first microprocessor is for general purpose and a second processor is for graphic processing purpose, comprising:

means for queuing all instructions at a first instruction queue;

means for distributing non graphic related instructions to be queued at a second instruction queue where said first microprocessor executes queued instructions from; and

means for distributing graphic related instructions to be queued at a third instruction queue where said second microprocessor executes queued instructions from.